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Original research paper

PROTON IRRADIATION EFFECTS ON SINGLE-PHOTON AVALANCHE DIODES*

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Abstract. *In this paper, we investigated the discrete switching of the Dark Count Rate between two or more levels in Single-Photon Avalanche Diode devices. This phenomenon, known as Random Telegraph Signal, is related to the density and distribution of defects in the semiconductor lattice and oxides. In this paper, we focused on a test chip containing SPADs with different architectures designed and implemented in 150-nm CMOS technology. The occurrence probability of the Random Telegraph Signal for proton-irradiated devices has been measured as a function of temperature for different SPAD layouts.*

Key words: *Single-photon avalanche diode, displacement damage, random telegraph signal, dark count rate, CMOS technology, proton irradiation*

1. INTRODUCTION

Nowadays, Single-Photon Avalanche Diodes (SPAD) [1] are widely employed in high-energy experiments, in astrophysics, in positron emission tomography (PET) [2], and in other applications.

They represent a valid solution capable of measuring a photon's arrival time with a resolution better than a few hundred picoseconds, as required in many applications. CCDs are unable to provide accurate measurements of low-intensity and fast transients, as for the optical counterparts of a high-energy gamma ray burst. Another important application, which requires sub-nanosecond time resolution, is the 3D scene reconstruction through Time-of-Flight (TOF) measurement of a laser pulse returning to the detector [4]. TOF-based systems are spreading in several fields of automotive and safety applications.

SPADs are, basically, p-n junctions biased above the breakdown voltage. In such conditions, the electric field is high enough to allow a single charge carrier, injected in the depletion layer, to trigger a self-sustaining avalanche.

A single photon can generate the charge carrier responsible for an avalanche current of the order of hundreds of milliamps in the depletion region. The rising edge of the signal is very fast, marking photon arrival time with extraordinary time resolution. The current continues to flow until the avalanche is quenched by lowering the bias voltage below the breakdown. The circuit performing such operation is referred to as a quenching circuit [5]. The SPAD detection principle based on avalanche formation results in an internal gain of the order of 10^6 that allows a reduction of complexity in the front-end amplification readout.

Since 2003, SPAD junctions have been integrated with complementary metal-oxide semiconductor (CMOS) electronics [6]. This allowed engineered electric fields and dedicated annealing steps and processes aimed at minimizing lattice damage to get better noise performances. Before that, SPADs were fabricated uniquely using a full custom process.

The CMOS SPAD allows to implement active quenching circuits, in-pixel read-out and processing electronics.

Nowadays, small-area SPADs can be fabricated in deep-submicron CMOS processes to create dense high-resolution arrays [7] where the same chip contains quenching electronics, analog sensing, and circuitry implementing photon counting and photon timing.

A major problem of CMOS-fabricated SPADs is the high dark count rate (DCR) level introduced by high doping levels and impurities in the processing steps. The aim of this paper is a better understanding of the DCR in a 150-nm CMOS fabrication process and of the dependence of DCRs on SPAD implementation design.

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DCR in SPAD devices could be also increase in a proton-rich environment as reported by [8][9].

2. Dark Count Rate

DCRs are mainly due to defects introduced in the semiconductor lattice and oxides during the technologic process and to the defects induced by radiations in silicon structure. These defects cause the generation of carriers in depletion regions through thermal processes (Shockley Read Hall generation, SRH) and tunneling processes (Trap Assisted Tunneling, TAT, and Band-To-Band Tunneling, BTBT). If thermal carrier generation depends on temperature profile, tunneling generation depends on electric field in SPAD junction.

The DCR due to all contributions is given by:

$$DCR_{TOT} = DCR_{SRH} + DCR_{TAT} + DCR_{BTBT} \quad (1)$$

2.1. Shockley-Read-Hall

In silicon devices thermally excited electrons can move from the valence band to the conduction band resulting in the generation of charge current. Such transitions are rare at working temperature due to the large and indirect bandgap of silicon. However, trap levels introduced in the bandgap by defects can act as intermediate state and facilitate the transition between conduction and valence band. This process, known as Shockley Read-Hall process, enhances the rate of carrier generation in semiconductor devices.

The SRH generation rate due to trapped levels in bandgap is

$$G_{SRH} = \frac{n_i^2 - pn}{\tau_{e0}\left(p + n_i e^{\frac{-(E_t - E_0)}{kT}}\right) + \tau_{h0}\left(n + n_i e^{\frac{-(E_t - E_0)}{kT}}\right)} \quad (2)$$

in which n_i is the intrinsic carrier concentration, n and p electron and hole concentrations, E_τ the trap level energy, E_0 the Fermi level, k the Boltzmann's constant, T the absolute temperature, τ_{e0} and τ_{h0} the lifetimes respectively of electrons and holes.

DCR due to SRH generation is obtained by integrating on depletion region (W_D) G_{SRH} times the probability for an electron-hole to trigger an avalanche (P_{BD}):

$$DCR_{SRH} = S\int_0^{W_D} G_{SRH} \cdot P_{BD}(z)dz \quad (3)$$

with *S* the surface of photodiode.

2.2. Tunneling

At high electric field, the carrier generation is increased by tunneling of electron from trap level into conduction band, known as Trap Assisted Tunneling, and from valence to conduction band, known as Band-To-Band Tunneling. TAT contribution is taken into consideration by introducing the function Γ resulting in:

$$G_{SRH\ TAT} = \frac{(n_i^2 - pn)(1+\Gamma)}{\tau_{e0}\left(p + n_i e^{\frac{-(E_t - E_0)}{kT}}\right) + \tau_{h0}\left(n + n_i e^{\frac{(E_t - E_0)}{kT}}\right)} \quad (4)$$

where Γ is defined as field-effect enhancement factor, since it depends on the local electric field.

The probability of tunnel is highly dependent on depletion thickness, electric field intensity and doping concentrations.

If the electric field intensity in avalanche region is higher than $7 \cdot 10^5 V/cm$, electrons are able to penetrate directly from valence into conduction band (BTBT).

The generation rate due to BTBT is given by:

$$G_{BTBT} = B \cdot E(z)^{5/2} \cdot D \cdot e^{-\frac{F_0}{E(z)}} \quad (5)$$

where B is a constant, $E(z)$ is the electric field intensity, D is 1 in depletion region in which tunneling effect occurs, while it is 0 on the edges of depletion region and F_0 is a constant depending on the form of the potential barrier in the forbidden band.

Similarly to SRH, DCR due to tunneling is obtained by

$$DCR_{TAT\ BTBT} = S\int_0^{W_D} G_{TAT\ BTBT} \cdot P_{BD}(z)\,dz \quad (6)$$

3. Random Telegraph Signal of DCR

In very small electronic devices, where only a few carriers are involved, individual defect sites or clusters of defects, which are responsible for DCR, may also give rise to a discrete switching between two or more DCR levels. This phenomenon is called Random Telegraph Signal (RTS).

The RTS could limit the use of SPADs in radiation environments as in space and in high-energy physics applications, since requinring continuous re-calibrations. This work aims to a better understanding of the phenomenon in order to develop special design and fabrication rules able to suppress DCR and RTS in CMOS SPAD technologies.

In the last two decades, RTS has been investigated in image sensors like Charged Coupled Devices [10]-[12] and Active Pixel Sensors [13]-[14].

RTS effect has been observed for first time in proton-irradiated SPADs in [15].

For such devices, RTS has been associated to metastable centers located in the silicon bulk.

RTS in SPAD DCR levels has been also reported in [16] for proton irradiated SPADs fabricated in 150-nm CMOS technology. Here we will further discuss a possible hypothesis for the observed RTS behaviour.

4. Chip Description

In this paper, we tested SPAD devices with two different structures, designed and implemented in a 150-nm process [17], [18]. The first structure is formed by a P+/Nwell junction with a guard ring obtained by blocking both Pwell and Nwell at the borders of the junction with a deep Nwell implantation (Fig. 1).

In this way, a low-doped ring surrounds the junction, avoiding a premature periphery breakdown.

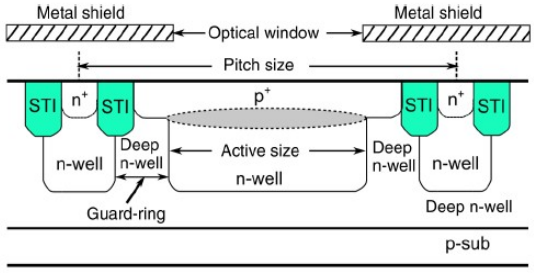

Figure 1. P+/Nwell SPAD structure (see [18])

In the second structure (Fig. 2), the active area is a Pwell/Niso junction. The guard ring is formed by avoiding well implantation at the junction periphery. A poly-Si gate blocks P+ implantation by avoiding contact with the shallow-trench-isolation (STI) region.

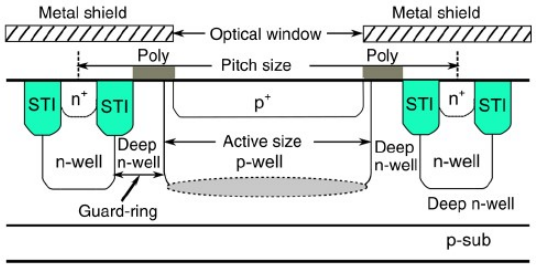

Figure 2. Pwell/Niso SPAD structure (see [18])

The test-chip contains different SPADs active region size (5, 10, 15, 20 μm) for each structure. Different breakdown voltages have been evaluated for two structures: 16.8 V for PN and 24.1 V for PWNISO.

More details on this device's characteristics can be found in [18].

Each SPAD of the array is integrated with its relative front-end pixel circuitry (Fig. 3): the SPAD is connected to a quenching transistor M2 acting as a resistor whose value can be adjusted by the gate tension $\mathbf{V}_{BQ}$. The transistor M1 is used to pull the SPAD below the breakdown voltage and disable its functionality. A clamping transistor M3 limits the pulse voltage of the SPAD to a maximum of 1.8 V to protect the subsequent digital electronics. The comparator digitalizes the SPAD pulse from M3 by comparing it to a reference voltage $\mathbf{V}_{REF}$ (set to 0.4 V), giving a 3.3 V digital output signal. Each SPAD can be individually selected through a row and column decoder and all SPADs share the same output through a multiplexer.

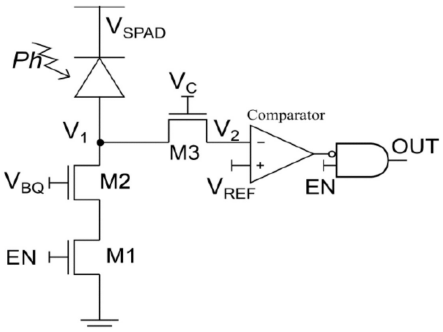

Figure 3. Pixel read-out circuit

5. Proton Irradiation Test Beam

The irradiation of two SPAD chips has been performed at the Laboratori Nazionali del Sud (LNS) in Catania by means of the "MP" tandem accelerator. The MP tandem, produced by the High Voltage Engineering Corporation, can accelerate ions from protons to gold with a 14 MV maximal terminal voltage.

The irradiation test has been performed with a proton beam of 24 MeV extracted in air through a 50 μm kapton window. A pneumatic beam stopper has been mounted in front of the kapton window, allowing the remote control of the beam.

In order to monitor the proton beam intensity during the test, an ionization chamber (IC) has been placed between the output window and the pneumatic beam stopper (Fig. 4).

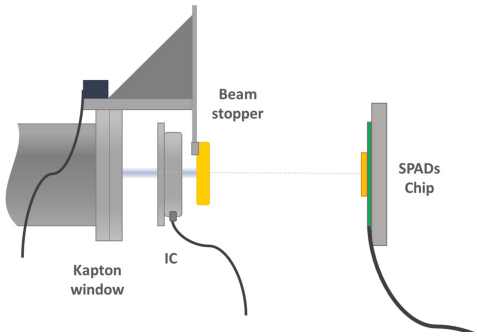

Figure 4. Layout of test beam setup

The IC, polarized with a voltage of about 800 V, provided an output current signal related to the intensity of the beam that crossed it. The relation between the IC signal and the proton beam current has been obtained by calibrating the IC with a Faraday cup. Fig. 5 shows the IC, the beam stopper, and the DUT along the proton beam-line.

In order to measure the beam intensity profile, a Gafchromic film (EBT3 type [19]) has been placed at the DUT position and irradiated in the same irradiation conditions of the chip.

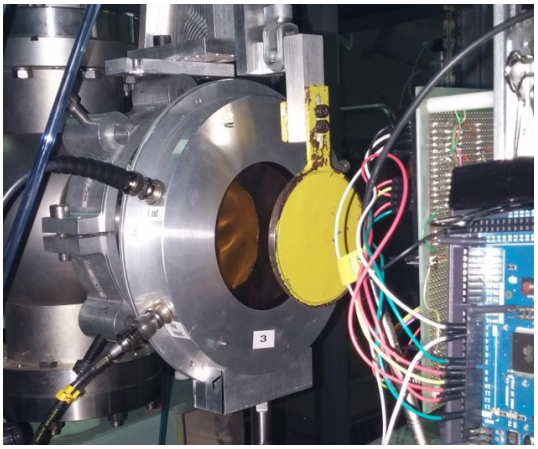

Figure 5. Test beam setup at LNS

The beam profile has been obtained on the GAF and, from its image analysis, it has been possible to estimate that the non-uniformity of the beam intensity on the surface where the chip is located is below 10% (Fig. 6).

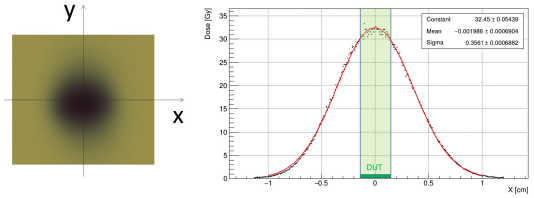

Figure 6. Exposed GAF and proton beam profile

The proton energy on the DUT has been estimated through the FLUKA simulation package. The simulation computed the energy losses in the kapton exit window of the beam-line, in the ionization chamber materials, and in the air. A mean energy of 20.5 MeV has been estimated.

5.1. Displacement Damage

Displacement damage occurs when a bulk atom is displaced from its lattice site. The recoil atom is then called a primary knock-on atom (PKA). As a consequence of displacement, a Vacancy (V) and an Interstitial (I) are produced (Fig. 7).

A vacancy is the absence of an atom from its normal lattice position. If this displaced atom moves into a non-lattice position, the resulting defect is called an interstitial. The combination of a vacancy and an adjacent interstitial is known as a Frenkel pair. Such a one-atom disorder in a crystalline lattice is called a "point defect".

Depending on the interaction process, the PKA can have enough energy to cause further displacements. In this case, a dense agglomerate of defects, noted as "cluster defects", could be formed.

Interstitials and vacancies are very mobile in a silicon lattice at room temperature. Some Frenkel pairs annihilate and no damage remains; the residual pairs migrate through the silicon lattice performing numerous reactions with each other and with impurity atoms in the silicon, producing the so-called secondary defects. This mechanism produces the real damage of silicon bulk material.

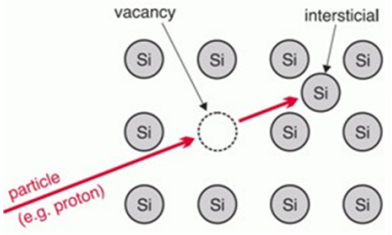

Figure 7. Vacancy and Interstitial formation in silicon

The displacement lattice damage in semiconductor devices can have a significant impact on their electrical properties. The radiation induced defects are responsible for the formation of energy levels inside the band-gap; these energy levels facilitate the transition of electrons and holes between the valence and the conduction band, resulting, as a major effect, in an increased dark current level in the device.

The silicon damage effect is quantified by the Displacement Damage Dose (DDD), which is expressed in terms of Non-Ionizing Energy Loss (NIEL) or displacement damage stopping power through the relation:

$$DDD[MeV/g] = NIEL \cdot \Phi \qquad (7)$$

where Φ is the particle fluence (expressed in particle·cm^{-2}) and the NIEL is expressed in MeV·cm^2/g. The NIEL is dependent on the incoming particle type and its energy.

The Displacement Damage Dose evaluated for two irradiated SPADs is reported in Table. 1.

Table 1. DDD delivered in proton irradiation to the tested devices

Chip	Run	Fluence (Protons/cm^2)	Energy (MeV)	DDD (TeV/g)
4	1	$9.1 \cdot 10^{10}$	21	608
5	1	$1.8 \cdot 10^{10}$	21	120
5	2	$5.6 \cdot 10^{10}$	21	376

6. SPAD Measurement Setup

The measurements of the DCR have been performed in a dark environment at room temperature. A motherboard provided the power supply to the chip read-out circuit and to the SPAD. The chip output signal is sent to an oscilloscope and to a digital counter. In order to enable and read out a certain pixel, a serial digital pattern is sent to the on-chip MUX by means of an external Arduino micro-controller. The SPAD power supply, provided by Hewlett Packard 6634A, digital counter, and Arduino have been connected via a serial bus to a computer and they are driven by the fully automated LABVIEW software. More details on the experimental setup can be found in [20].

7. RTS Observation

The measurements of DCR after proton irradiation show an average increase of almost one order of magnitude (Fig. 7). This indicates that many defects have been introduced after the delivered proton fluence.

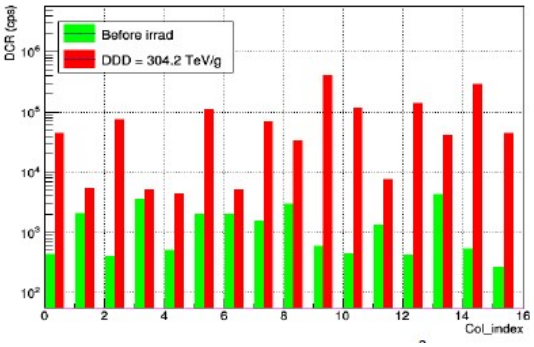

Figure 7. DCR increase after irradiation in 10x10-μm SPAD arrays

In order to investigate the presence of RTS before and after irradiation, three hours of continuous DCR measurements have been performed for each single SPAD belonging to a large sample containing the two SPAD layouts described in Sec. 3.

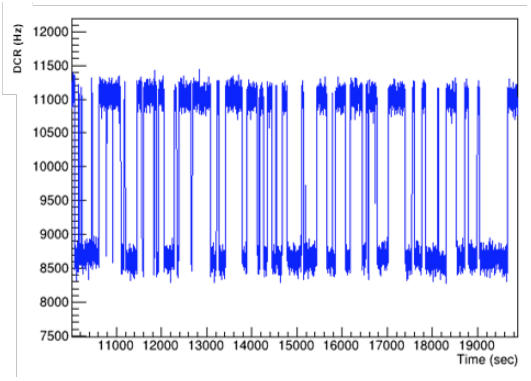

Figure 8. Two-level DCR fluctuations

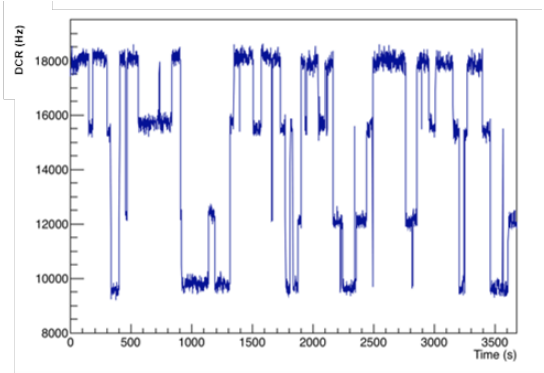

Figure 9. Multi-level DCR fluctuations

Table 2. RTS observation in two different SPAD layouts

Layout	Total SPADs	RTS pixels	Two-level RTS	Multi-level RTS	RTS fraction
P+/Nwell	132	105	11	94	80%
Pwell/Niso	140	67	14	53	48%

Before irradiation, a small fraction of SPAD (about 5%) showed some discrete fluctuations of the DCR. After irradiation, a very large fraction (Tab. 2) of irradiated SPAD showed an occurrence of RTS in DCR levels. For some pixels, two-level DCR fluctuations have been observed (Fig. 8) while many others exhibited multi-level DCR fluctuations (Fig. 9). Table 2 summarizes the fraction of the observed RTS in two different SPAD layouts.

The higher probability of finding RTS fluctuations in P+/Nwell layouts could be explained by the higher doping profile in these layouts as compared to the Pwell/Niso one. The defects introduced by irradiations probably combine with elements used for the doping process and, in some way that is still unclear, could create complex and metastable defects which produce the RTS effect.

Focusing our attention on two-level RTS pixels, we measured the time spent in high and low DCR values and we observed an exponential time distribution (Fig. 10). This is foreseen by a Poisson distribution of random switching events [21].

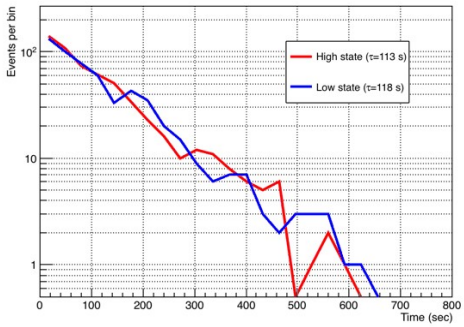

Figure 10. Time spent in a high and low DCR state in a SPAD with a two-level RTS fluctuations

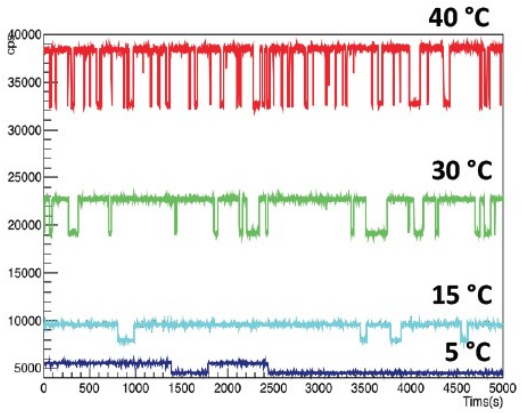

Figure 11. Temperature dependence of the RTS occurrence probability

The time constant of such exponential distribution is related to the RTS occurrence probability. By studying SPAD, showing RTS as function of the temperature, we observed a dependence on the temperature of the RTS occurrence probability (Fig. 11).

The trend of the time constant has been investigated here for the two structures by performing long-time measurements of DCR in a climatic chamber in the temperature range of 5°C–45°C. The time constants (τ_{up}, τ_{down}) have been found to follow the law:

$$\frac{1}{\tau} = C\exp(-E_{act}/KT) \tag{8}$$

The measured time constants are reported in Fig. 12 and Fig. 13 for the high and low level, respectively. Each graph reports the measurement of a single two-level RTS found in P+/Nwell and Pwell/Niso layouts. For both structures, a value around *0.8–0.9* □□ has been found for the activation energy (Figs 12–13).

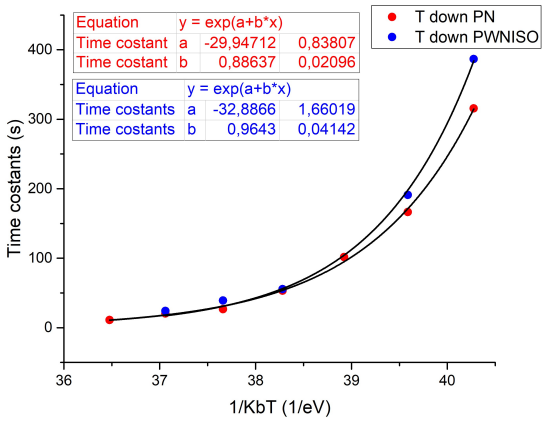

Figure 12. Time constants as a function of 1/KT for low RTS level in two SPAD pixels with a different layout

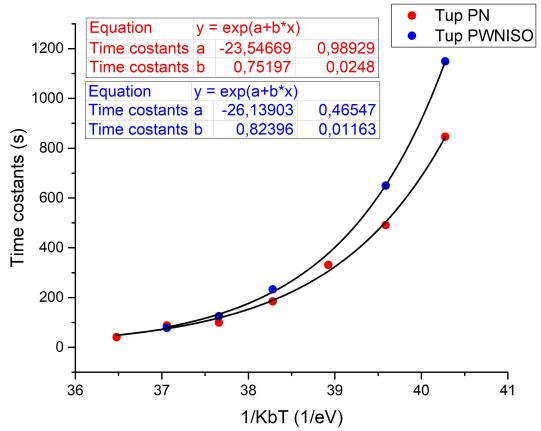

Figure 13. Time constants as a function of 1/KT for high RTS level in two SPAD pixels with a different layout

A phosphorus-vacancy center has been indicated as a possible explanation for the RTS behaviour ([9] and [11]). A dipole structure of such complex defect introduces a meta-stable state. A calculation reported in [19] estimated an activation energy value for this re-orientation mechanism of 0.93 eV.

The values we measured in this research for the time constant activation energy for both SPAD layouts are very similar to the one calculated in [22]. We consider this a strong indication that P-V center defects could be the main factor responsible for RTS.

8. Conclusion

This paper reports the proton irradiation effect on Single-Photon Avalanche Diodes implemented in 150-nm CMOS technology. The device has been irradiated with a 21-MeV proton beam at the Tandem accelerator at LNS INFN in Catania (Italy).

We clearly observed that the RTS occurrence probability depends on the SPAD implementation layout. The RTS mechanism has been analysed by means of studying RTS time constants as a function of temperature. The measurements reported in this work could support the hypothesis that attributes the RTS behaviour to the reorientation of the phosphor-vacancy (P-V) center.

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